## ■ OVERVIEW

The SM5624N Series is a range of quartz oscillator module ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a low-voltage, low-current oscillator circuit and output buffer. The ICs incorporate oscillation capacitors having excellent frequency characteristics, and thus ensures stable oscillation of a quatz fundamental wave without connecting any external components.

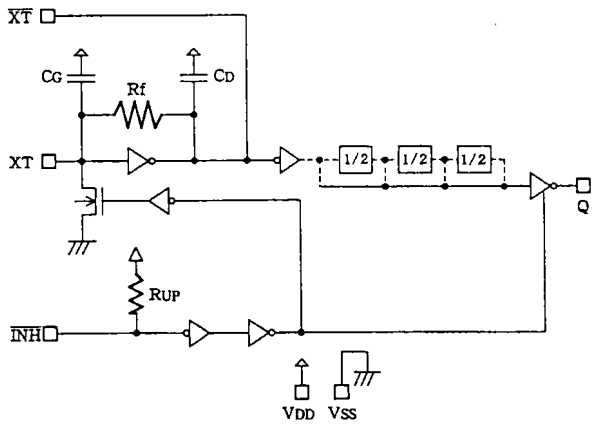
## ■ FEATURES

- Up to 30 MHz frequency
- Fundamental wave
- Design optimized for a supply voltage of 2.7 to 3.6 V (operating voltage 2.7 to 5.5V)
- Built-in feedback resistor in inverter amplifier
- Chip form
- Molybedenum-gate CMOS construction
- Low current consumption
- Built-in oscillation capacitors CG and CD
- Output tristate functin
- Low current consumption
- Standby function (Standby: oscillation stop, output high impedance).

## ■ PIN DESCRIPTION

| Name | Function |
|---|---|
| XT | Oscillation input |
| $\overline{XT}$ | Oscillation output |
| $\overline{INH}$ | "L": oscillation stop, output hihg impedance, internal pull-up resistor (Pull-up resistance changes tolimit the standy current) |
| $V_{DD}$ | Supply voltage |
| $V_{SS}$ | Ground |
| Q | Output pin |

## ■ BLOCK DIAGRAM



## ■ SERIES LINEUP

| Version | Output |
|---|---|
| SM5624 N1 | fo |
| N3 | fo/2 |
| N5 | fo/4 |
| N7 | fo/8 |

fo: fundamental frequency

## ■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}$ = 0V)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | -0.5 to +7.0 | V |
| Input voltage | $V_{IN}$ | -0.5 to $V_{DD}$ +0.5 | V |
| Output voltage | $V_{OUT}$ | -0.5 to $V_{DD}$ +0.5 | V |
| Storage temperature | $T_{STG}$ | -65 to +150 | °C |
| Output current | $I_{OUT}$ | 25 | mA |

## ■ RECOMMENDED OPERATING CONDITIONS

($V_{SS}$ = 0V)

| Item | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 2.7 | | 3.6 | V |
| Input voltage | $V_{IN}$ | $V_{SS}$ | | $V_{DD}$ | V |
| Operating temperature | $T_{OPR}$ | -20 | | +80 | °C |

## ■ ELECTRICAL CHARACTERISTICS

($V_{DD}$ =2.7 to 5.5V, $V_{SS}$ = 0 V and Ta= -20 to +80°C unless otherwise noted.)

| ITEM | SYMBOL | CONDITIONS | | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|---|
| H-level output voltage | $V_{OH}$ | Q pin, Fig. 1 | $V_{DD}$=4.5V. $I_{OH}$=16.0mA | 4.0 | 4.2 | | V |
| | | | $V_{DD}$=2.7V. $I_{OH}$=8mA | 2.2 | 2.4 | | |
| L-level output voltage | $V_{OL}$ | Q pin, Fig. 1 | $V_{DD}$=4.5V. $I_{OL}$=16.0mA | | 0.3 | 0.4 | V |
| | | | $V_{DD}$=2.7V. $I_{OL}$=8mA | | 0.3 | 0.4 | |
| H-level input voltage | $V_{IH}$ | $\overline{INH}$ pin | | 0.7$V_{DD}$ | | | V |
| L-level input voltage | $V_{IL}$ | $\overline{NH}$ pin | | | | 0.3$V_{DD}$ | V |
| Current consumption | $I_{DD1}$ | Fig. 2 $\overline{INH}$=OPEN $C_L$=15pF, f=30MHz, $V_{DD}$=3±0.3V | SM5624N1 | | 6 | 12 | mA |
| | | | SM5624N3 | | 4 | 8 | |
| | | | SM5624N5 | | 3 | 6 | |
| | | | SM5624N7 | | 2 | 4 | |
| | | Fig. 2 $\overline{INH}$=OPEN $C_L$=15pF, f=30MHz, $V_{DD}$=5±0.5V | SM5624N1 | | 12 | 24 | |
| | | | SM5624N3 | | 8 | 16 | |
| | | | SM5624N5 | | 6 | 12 | |
| | | | SM5624N7 | | 5 | 10 | |
| Standby current | $I_{ST}$ | Fig. 2, $\overline{INH}$="L" | $V_{DD}$=3±0.3V | | 1.5 | 6 | |
| | | | $V_{DD}$=5±0.5V | | 4 | 15 | µA |
| $\overline{INH}$ pin pull-up resistance | $R_{UP1}$ | Fig. 3 | $\overline{INH}$=Vss, $V_{DD}$=3.6V | 2 | | 15 | MΩ |
| | $R_{UP2}$ | | $\overline{INH}$=2.7V, $V_{DD}$=3.6VV | 50 | | 300 | kΩ |
| Feedback resistance | $R_f$ | Fig. 4 | | 1.0 | | 10 | MΩ |
| Internal capacitor | $C_G$ | Design value | | 18 | 20 | 22 | pF |
| | $C_D$ | | | 18 | 20 | 22 | |

## ■ SWITCHING CHARACTERISTICS

Vss =0V and Ta= -20 to +80°C unless otherwise noted.

| ITEM | SYMBOL | CONDITIONS | | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output rise time | $T_{r1}$ | Fig. 5 0.1$V_{DD}$ to 0.9$V_{DD}$ | $V_{DD}$=5±0.3V, $C_L$=15pF | | 2 | 4 | ns |
| | $T_{r2}$ | | $V_{DD}$=5±0.5V, $C_L$=15pF | | 1.5 | 3 | |
| | $T_{r3}$ | | $V_{DD}$=5±0.3V, $C_L$=30pF | | 3 | 6 | |
| | $T_{r4}$ | | $V_{DD}$=5±0.5V, $C_L$=50pF | | 4 | 8 | |
| Output fall time | $T_{f1}$ | Fig. 5 0.9$V_{DD}$ to 0.1$V_{DD}$ | $V_{DD}$=5±0.3V, $C_L$=15pF | | 2 | 4 | ns |
| | $T_{f2}$ | | $V_{DD}$=5±0.5V, $C_L$=15pF | | 1.5 | 3 | |
| | $T_{f3}$ | | $V_{DD}$=5±0.3V, $C_L$=30pF | | 3 | 6 | |
| | $T_{f4}$ | | $V_{DD}$=5±0.5V, $C_L$=50pF | | 4 | 8 | |
| Output duty cycle | DUTY | Fig. 5, $C_L$=15pF f=30MHz, Ta=25°C | $V_{DD}$=3.0V | 45 | | 55 | % |
| | | | $V_{DD}$=5.0V | 40 | | 60 | |
| Output disable delay time | $T_{PLZ}$ | Fig. 5, Ta=25°C, $V_{DD}$=3.0V, load $C_L$≤30pF | | | | 150 | ns |
| Output enable delay time | $T_{PZL}$ | | | | | 150 | |
| Operaing frequency | f | Fig. 5, $C_L$=15pF, $V_{DD}$=2.7to 5.5V,*1 | | 30 | | | MHz |

* 1: Guaranteed by the lot monitoring

## ■ MEASURING CIRCUIT

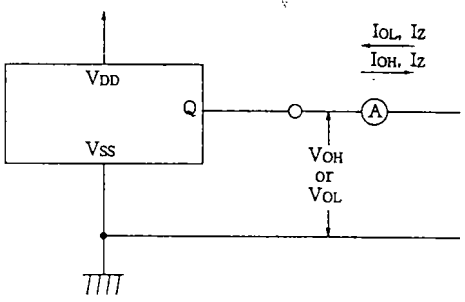



Figure 1

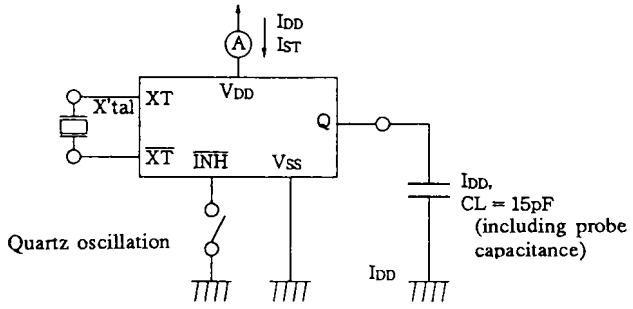
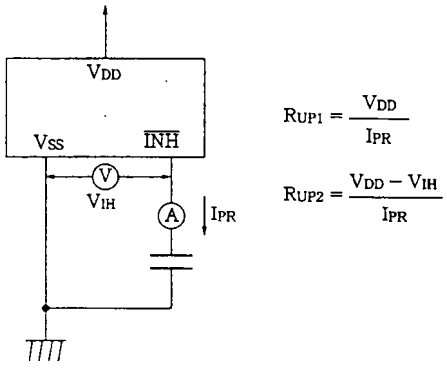



Figure 2




$$R_{UP1} = \frac{V_{DD}}{I_{PR}}$$

$$R_{UP2} = \frac{V_{DD} - V_{IH}}{I_{PR}}$$

Figure 3

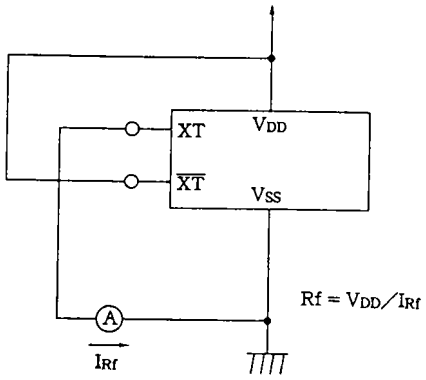
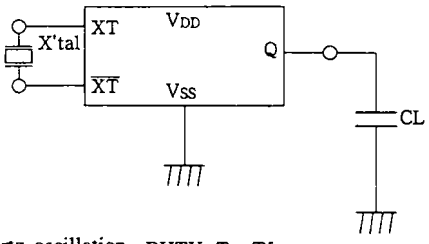


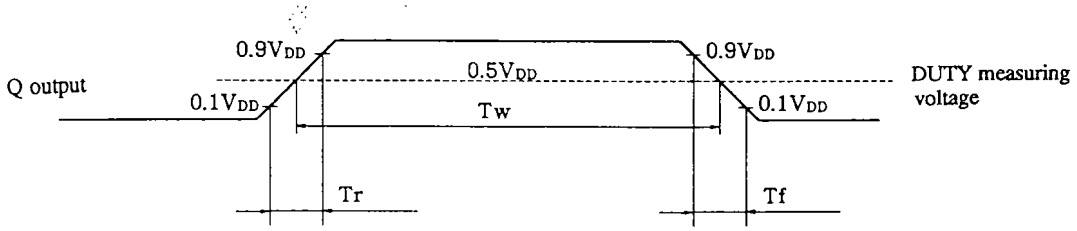

Figure 4



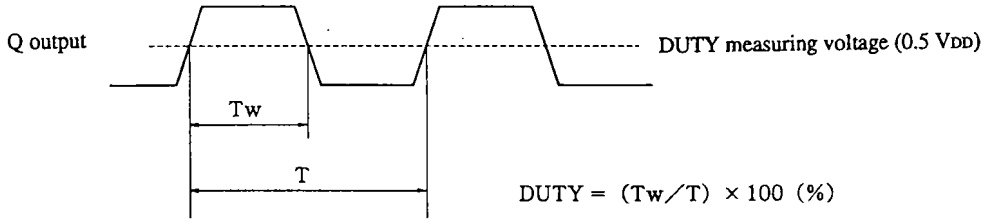

DUTY, $T_{r1,2}$, $T_{f1,2}$
$C_L$=15pF
$T_{r3}$, $T_{f3}$
$C_L$=30pF
Tr4, Tf4
$C_L$=50pF
($C_L$ includes probe capacitance)

Figure 5

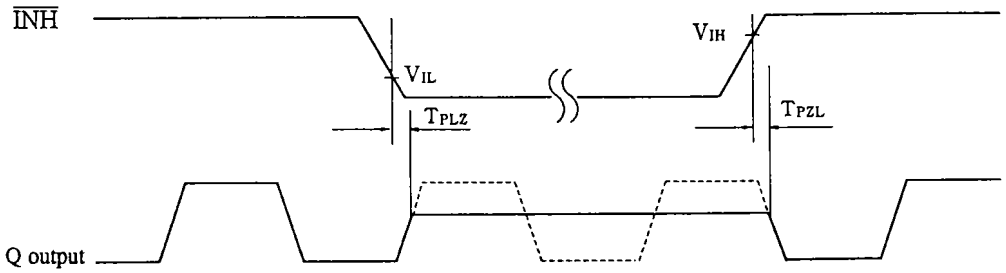
## ■ SWITCHING TIME MEASURING WAVEFORM




## ■ OUTPUT DUTY CYCLE TIME

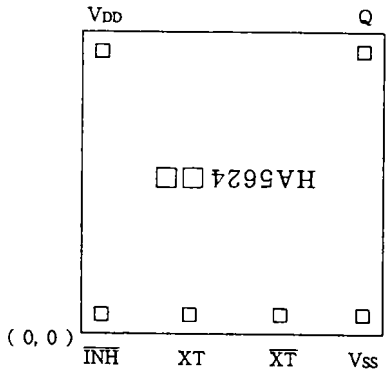



## ■ OUTPUT DISABLE DELAY TIME, OUTPUT ENABLE DELAY TIME




$\overline{INH}$ input waveform Tr=Tf 10 ns or less

## ■ PAD LAYOUT




Chip size: 0.89 × 1.28mm
Chip thickness: 400±30 µm
Check back surface: $V_{DD}$ level

* □□ version name

## ■ PAD COORDINATES (Unit: µm)

| Pin name | X | Y |
|---|---|---|
| $\overline{INH}$ | 170 | 183 |
| XT | 360 | 183 |
| $\overline{XT}$ | 550 | 183 |
| $V_{SS}$ | 740 | 183 |
| Q | 743 | 1133 |
| $V_{DD}$ | 136 | 1133 |